LARGE-SIGNAL DESIGN OF MMMIC Ka-BAND POWER AMPLIFIERS BASED ON PHYSICAL MODELS.

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ABSTRACT

A quasi-two-dimensional physical model is used to predict the effects of process variations on the DC, small-, and large-signal behaviour of a pHEMT. A large-signal equivalent circuit model of the mm-wave pHEMT extracted from the physical model is used to predict the non-linear behaviour of an amplifier. A two-tone on-wafer source- and load-pull measurement system has been constructed to allow verification of the modelling procedure.

INTRODUCTION

Once a MMMIC has been fabricated it is almost impossible to change the values of the passive components or the lengths of the microstrip lines, and hence the design procedure should ideally lead to circuits that operate correctly first time. There is a random variation in every fabrication process and it is important to forecast the yield by predicting the deviation this random variation will cause in the behaviour of the MMMICs. In many cases the active devices will be operating in a non-linear region so the large-signal behaviour of the FETs must be accurately modelled.

This paper reports a design methodology that uses a quasi two-dimensional physical model [1] to predict the DC and small-signal behaviour of a pHEMT and a Harmonic Balance program using a non-linear equivalent circuit model of the FET to predict the large signal behaviour. This allows the process variations to be investigated and the design to be optimised for the specific process (yield-oriented design). A design of a 38 GHz MMIC power amplifier has been developed using this procedure.

NON-LINEAR CAD

The physical model, which is based on a quasi-two dimensional physical description, has been developed as a CAD tool that allows the prediction of the DC-IV curves and the S-parameters of a FET from a knowledge of the physical structure and the doping profile [1]. Ideally no DC or microwave measurements are required in this approach in order to accurately predict the FET's behaviour, subsequently no fitting of data need be performed. If the process variation in the doping and structure are known the physical model can calculate the variation in the behaviour of the FETs.

The H40 process (0.23μm gate length pHEMT) from GEC-Marconi Materials Technology (GMMT) at Caswell, UK is being used as the basis of the MMMIC designs. Figure 1 shown several DC-IV characteristics at V_{GS}=0V for a number of 6x60μm gate width pHEMTs together with the predicted variation from the model using the process variance (gate recess, doping densities, alloy composition, etc.). Figure 2 shows the measured and modelled S-parameters for V_{DS}=5V, I_D=I_{DSS}/2.

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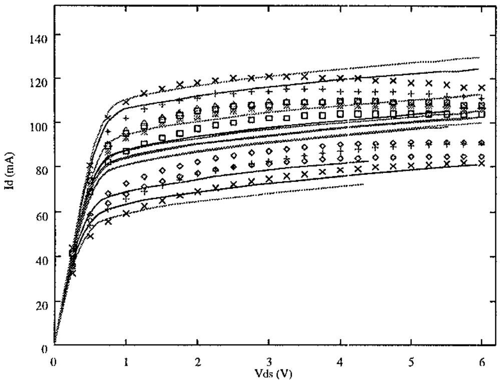

Figure 1: The range of VGS=0V DC-IV characteristics. The solid lines are predicted by the physical model, measured data is shown with discrete symbols.

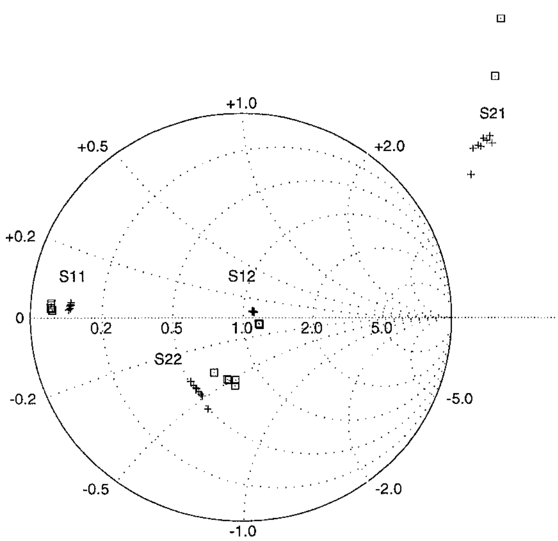

Figure 2: The range of S-parameters. The crosses are measured data, and the boxes are modelled values.

A large-signal equivalent circuit model (Figure 3) [2] can be extracted from the DC-IV curves and the small-signal S-parameters or directly from the physical model. The equivalent circuit model is used in a Harmonic Balance [3] program to predict the gain and intermodulation distortion as a function of input power, source, and load impedance.

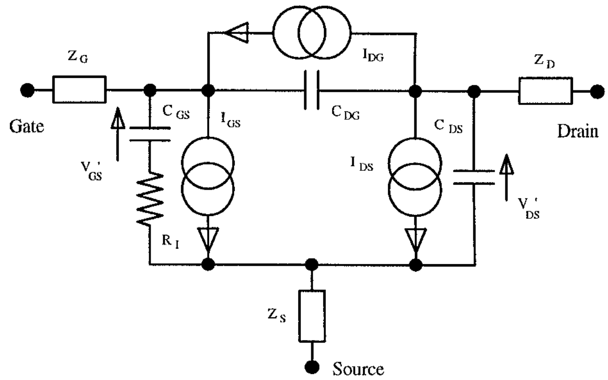

Figure 3: The large-signal equivalent circuit model of the pHEMT used in the Harmonic Balance program.

AMPLIFIER DESIGN

In order to validate the design procedure a three-stage balanced amplifier (Figure 4) was designed for operation at 38 GHz. The design uses lumped element inter-stage matching. The amplifier is designed to achieve 17 dBm output at the one dB gain compression point with a 38 GHz small-signal gain of 19 dB and a bandwidth of 3 dB. Figure 5 shows the predicted behaviour of the gain and input match over the range 26.5 to 40 GHz with the variance predicted by the physical model.

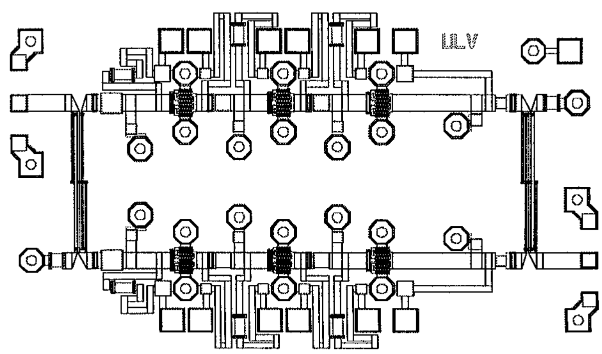

Figure 4: A schematic of the three-stage balanced amplifier. The input is on the left.

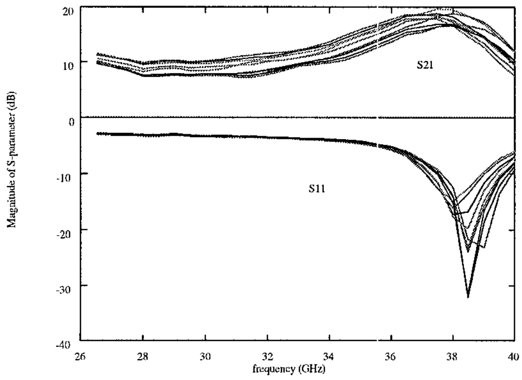

Figure 5: Predicted magnitudes of S11 and S21 for the three-stage balanced amplifier for several pHEMTs with typical process variations.

MEASUREMENT

A schematic of the two-tone source- and load-pull measurement system is shown in Figure 6. The source tuner is a slide-screw waveguide tuner, the load tuner is a variable attenuator and a moveable short. The maximum power into the device is 13 dBm at 26.5 GHz and 10 dBm at 38 GHz.

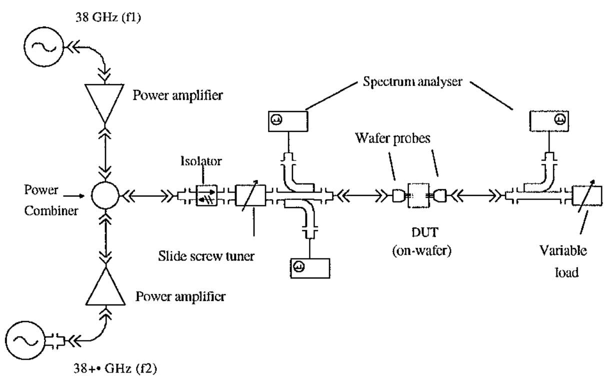

Figure 6: A Schematic of the on-wafer two-tone source- and load-pull measurement system.

Figure 7 shows a measurement of gain at 26.5 GHz as a function of input power for an H40 4x80 μm gate width FET (biased at V_D=2V, V_G=-0.5V) and the predicted gain compression from the Harmonic Balance program. Figure 8 shows the small-signal gain of an H40 6x60 μm gate width FET (biased at V_D=6V, I_D=I_{DSS}/2) at 27 GHz as a function of load impedance. Figure 9 shows a measurement of intermodulation distortion. The two input signals are at 26.50 and 26.51 GHz.

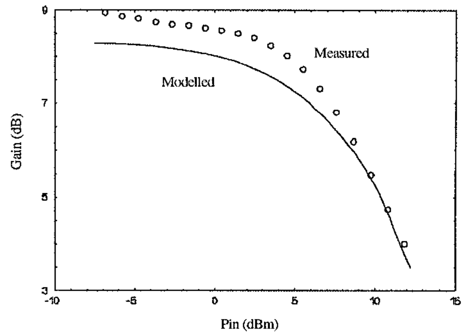

Figure 7: Comparison between the predicted and measured gain compression.

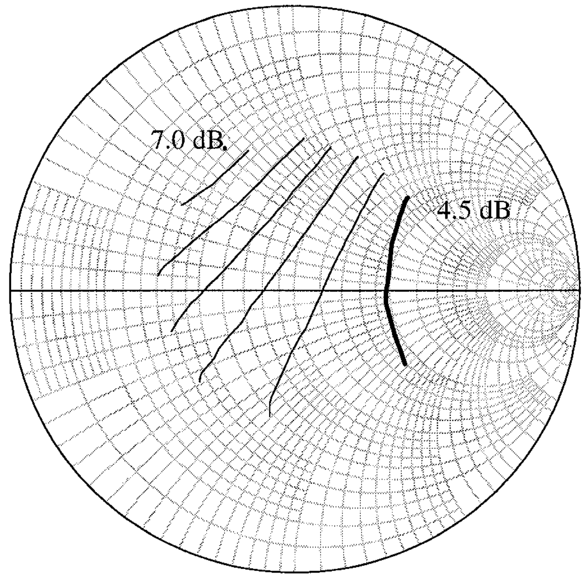

Figure 8: Contours of constant gain as a function of load impedance.

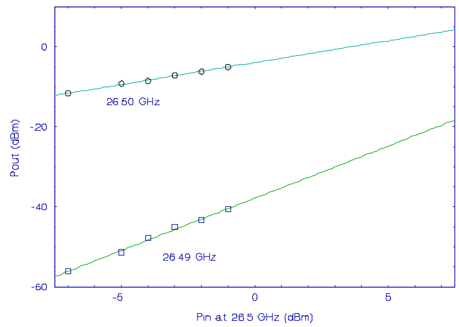

Figure 9: A preliminary measurement of the intermodulation distortion of the 6x60µm pHEMT

CONCLUSIONS

This paper describes a large-signal MMMIC design methodology that allows accurate predictions of the small- and large-signal behaviour of FETs and accounts for fabrication process variations. A 38 GHz pHEMT power amplifier has been designed using this approach. A new on-wafer mm-wave automated load-pull and intermodulation distortion measurement system has been developed.

REFERENCES

[1] R.Drury and C.M.Snowden, "A Quasi-Two-Dimensional HEMT Model for Microwave CAD Applications." IEEE Trans **ED-42**, (1995) pp 1026-1032.

[2] R.R.Pantoja, M.J.Howes, J.R.Richardson, and C.M.Snowden, "A Large-Signal Physical MESFET Model for Computer-Aided Design and Its Applications." IEEE Trans **MTT-37**, (1989) pp 2039-2045.

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